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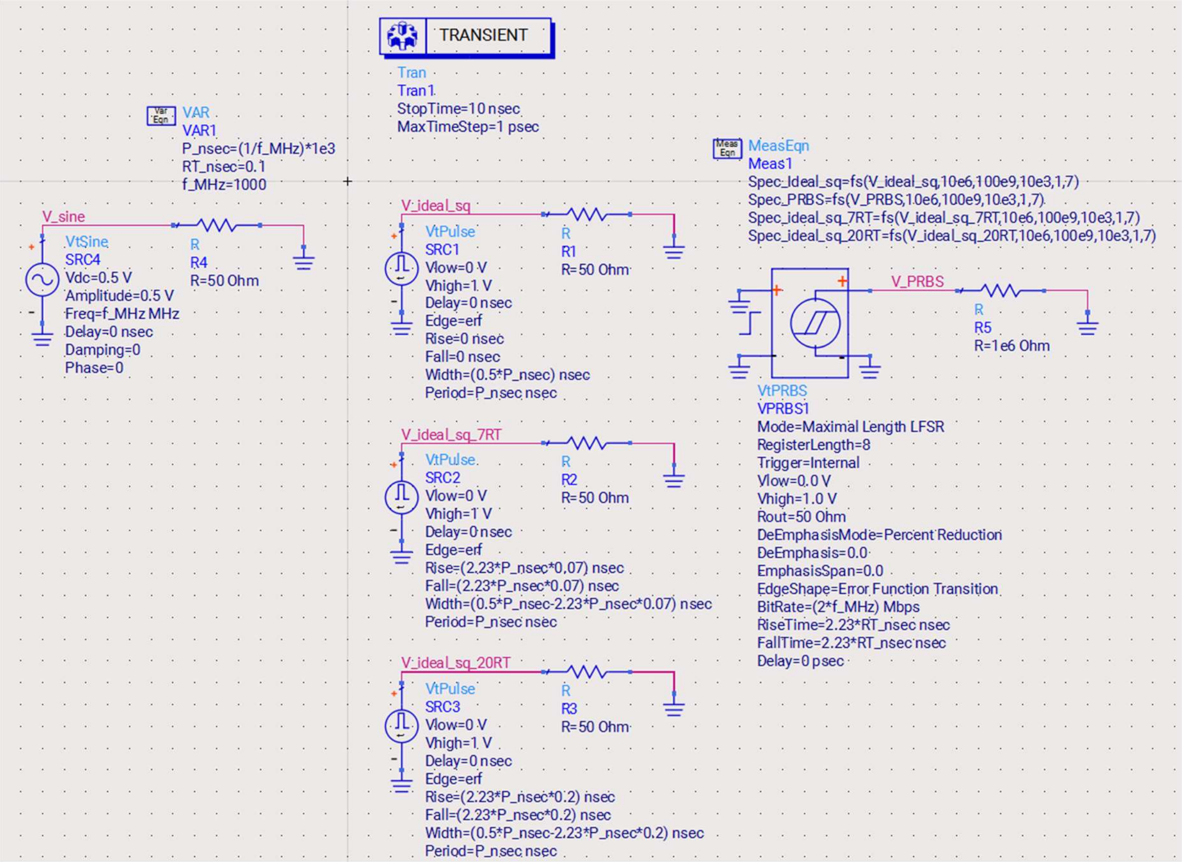
Week 3 Labs
2026-01-26

Lab 1:

The purpose of this lab was to learn the skill of creating Fourier transforms in ADS and to explore the manifestation of harmonics for various types of square waves.

I analyzed an ideal square wave, two square waves with different rise times (RT) (7% and 20%), and a pseudo-random bit sequence (PRBS) signal. Since ADS classifies the RT as the 0-100 RT, I modified the RT to make it the 10-90 RT. I also shortened the width by the same amount to account for the RT so that the duty cycle remained at 50%.



Tran
Tran1
StopTime=10 nsec
MaxTimeStep=1 psec

VAR
VAR1
P_nsec=(1/f_MHz)*1e3
RT_nsec=0.1
f_MHz=1000

MeasEqn
Meas1
Spec_Ideal_sq=fs(V_ideal_sq,10e6,100e9,10e3,1,7)
Spec_PRBS=fs(V_PRBS,10e6,100e9,10e3,1,7)
Spec_ideal_sq_7RT=fs(V_ideal_sq_7RT,10e6,100e9,10e3,1,7)
Spec_ideal_sq_20RT=fs(V_ideal_sq_20RT,10e6,100e9,10e3,1,7)

VtSine
SRC4
Vdc=0.5 V
Amplitude=0.5 V
Freq=f_MHz MHz
Delay=0 nsec
Damping=0
Phase=0

R
R4
R=50 Ohm

VtPulse
SRC1
Vlow=0 V
Vhigh=1 V
Delay=0 nsec
Edge=erf
Rise=0 nsec
Fall=0 nsec
Width=(0.5*P_nsec) nsec
Period=P_nsec nsec

R
R1
R=50 Ohm

VtPulse
SRC2
Vlow=0 V
Vhigh=1 V
Delay=0 nsec
Edge=erf
Rise=(2.23*P_nsec*0.07) nsec
Fall=(2.23*P_nsec*0.07) nsec
Width=(0.5*P_nsec-2.23*P_nsec*0.07) nsec
Period=P_nsec nsec

R
R2
R=50 Ohm

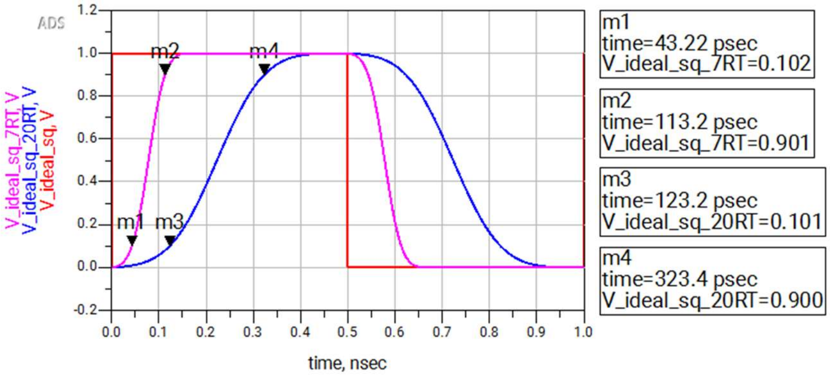
VtPulse
SRC3
Vlow=0 V
Vhigh=1 V
Delay=0 nsec
Edge=erf
Rise=(2.23*P_nsec*0.2) nsec
Fall=(2.23*P_nsec*0.2) nsec
Width=(0.5*P_nsec-2.23*P_nsec*0.2) nsec
Period=P_nsec nsec

R
R3
R=50 Ohm

VtPRBS
VPRBS1
Mode=Maximal Length LFSR
RegisterLength=8
Trigger=Internal
Vlow=0.0 V
Vhigh=1.0 V
Rout=50 Ohm
DeEmphasisMode=Percent Reduction
DeEmphasis=0.0
EmphasisSpan=0.0
EdgeShape=Error Function Transition
BitRate=(2*f_MHz) Mbps
RiseTime=2.23*RT_nsec nsec
FallTime=2.23*RT_nsec nsec
Delay=0 psec

R
R5
R=1e6 Ohm

Figure 1: Circuit modeled in ADS to simulate square waves with varying rise times and a PRBS signal for lab 1.



m1
time=43.22 psec
V_ideal_sq_7RT=0.102

m2
time=113.2 psec
V_ideal_sq_7RT=0.901

m3
time=123.2 psec
V_ideal_sq_20RT=0.101

m4
time=323.4 psec
V_ideal_sq_20RT=0.900

Figure 2: Rise times of the 7% RT square wave (pink, 70 nsec) and 20% RT square wave (blue, 200 nsec).

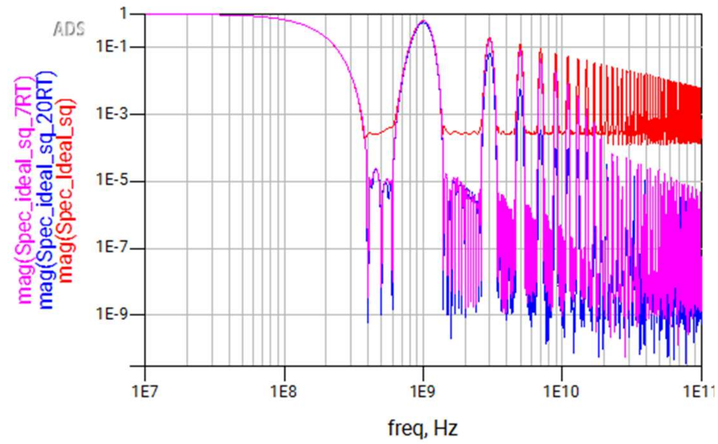


Figure 3: Fourier analysis of a square wave with 0% rise time (red), 7% rise time (pink), and 20% rise time (blue). The square wave has a greater magnitude of higher-order odd harmonics.

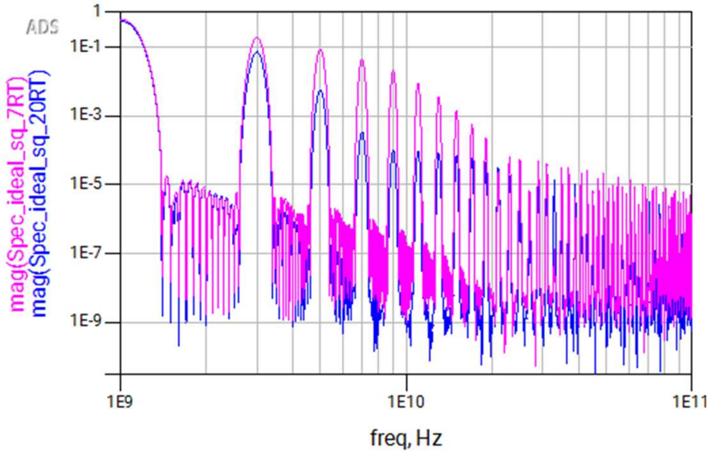


Figure 4: Comparison of Fourier analysis of square waves with a 7% rise time (pink) and a 20% rise time (blue). The lower-order odd harmonics have greater amplitude in the 7% case than in the 20% case.

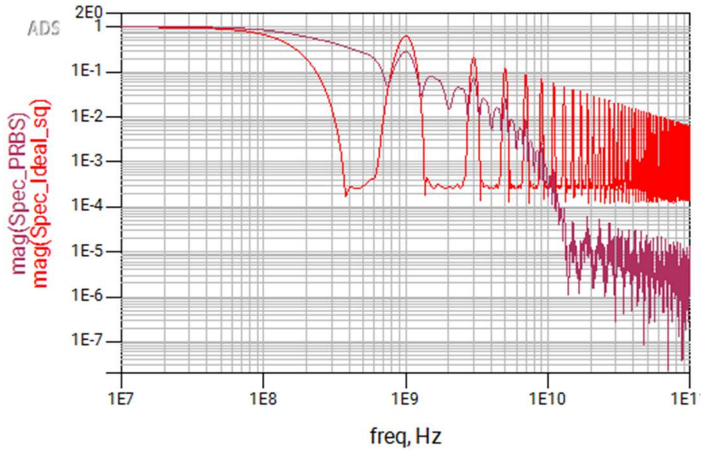


Figure 5: Fourier analysis of an ideal square wave (red) and of a PRBS signal (maroon). The amplitudes of the even harmonics of the PRBS signal are much greater than that of the ideal square wave.

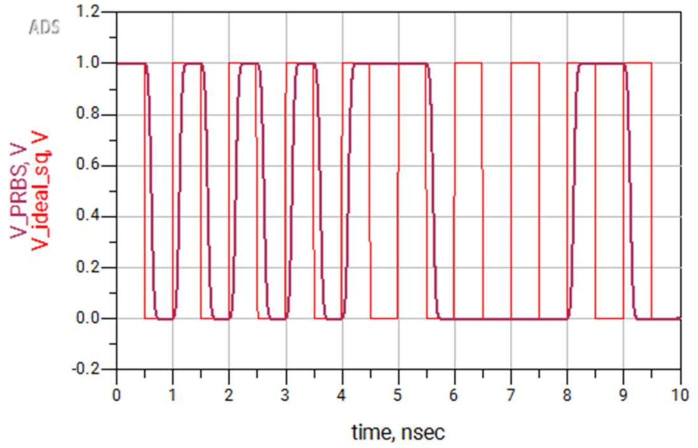


Figure 6: Transient analysis of the PRBS signal (maroon) overlayed on the ideal square wave (red) to demonstrate that the PRBS frequency is 2x that of the square wave and that the PRBS signal is not symmetrical.

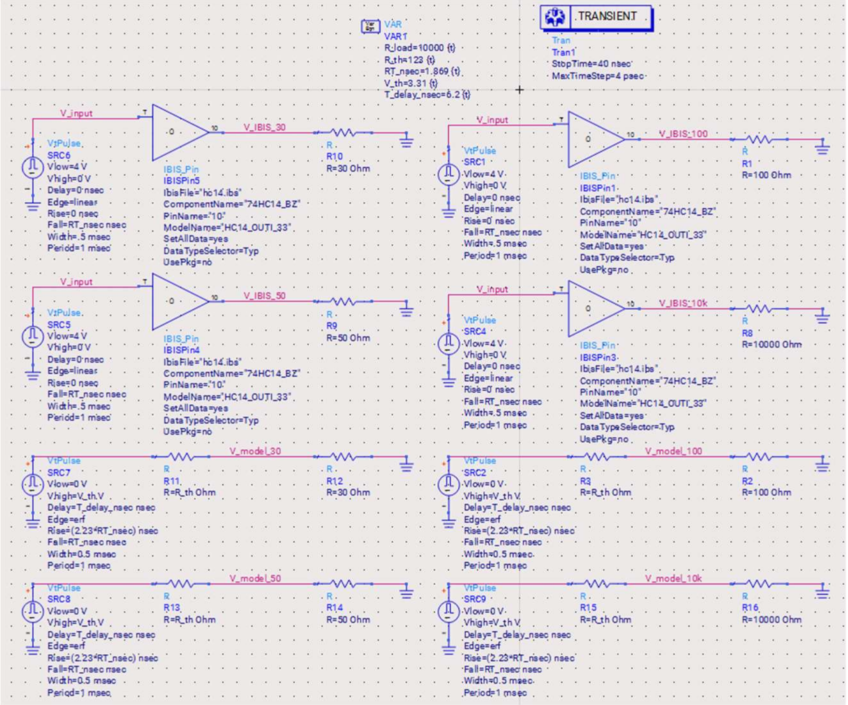
Based on the spectral analysis of these curves, it is clear that the ideal square wave has an infinite bandwidth because the higher frequency components never fall off. There is an argument to be made that it might not matter above 100 GHz because the harmonics above 100 GHz individually contribute to less than 1% of the total power.

Using the same cutoff power criteria, the highest bandwidth for the 7% and 20% rise times is roughly 9 GHz. It is challenging to say whether the bandwidth for the PRBS signal matters as much because what matters when reading bits is the value at the read time and not factors like rise time. For this reason, I would argue that the bandwidth of the PRBS is $2 * f_{clock} = 2\ GHz$.

So what: My takeaways are that as the rise time increases, the higher-order harmonics decrease in power. Another important takeaway is that a PRBS signal will express even harmonics since it's not symmetric. Finally, I learned how to tune parameters in ADS including rise/fall time (scaling from 0-100 to 10-90) an width (accounting for the rise/fall time) to match my intended waveforms.

Lab 2:

The purpose of this lab was to explore the differences between IBIS models and Thevenin models. With those discoveries, I inquired on the inaccuracy of the Thevenin model as compared to the IBIS model and judge its usefulness. Next, I explore the input capacitance of the IBIS model with an equivalent lumped circuit model with and without the package included.



```
VAR
VAR1
R_load=10000 {t}
R_th=123 {t}
RT_nsec=1.869 {t}
V_th=3.31 {t}
T_delay_nsec=6.2 {t}

TRANSIENT
Tran
Tran1
StopTime=40 nsec
MaxTimeStep=4 psec

VtPulse
SRC6
Vlow=4 V
Vhigh=0 V
Delay=0 nsec
Edge=linear
Rise=0 nsec
Fall=RT_nsec nsec
Width=.5 msec
Period=1 msec

IBIS_Pin
IBISPin5
IbisFile="hc14.ibs"
ComponentName="74HC14_BZ"
PinName="10"
ModelName="HC14_OUTI_33"
SetAllData=yes
DataTypeSelector=Typ
UsePkg=no

R
R10
R=30 Ohm

VtPulse
SRC1
Vlow=4 V
Vhigh=0 V
Delay=0 nsec
Edge=linear
Rise=0 nsec
Fall=RT_nsec nsec
Width=.5 msec
Period=1 msec

IBIS_Pin
IBISPin1
IbisFile="hc14.ibs"
ComponentName="74HC14_BZ"
PinName="10"
ModelName="HC14_OUTI_33"
SetAllData=yes
DataTypeSelector=Typ
UsePkg=no

R
R1
R=100 Ohm

VtPulse
SRC5
Vlow=4 V
Vhigh=0 V
Delay=0 nsec
Edge=linear
Rise=0 nsec
Fall=RT_nsec nsec
Width=.5 msec
Period=1 msec

IBIS_Pin
IBISPin4
IbisFile="hc14.ibs"
ComponentName="74HC14_BZ"
PinName="10"
ModelName="HC14_OUTI_33"
SetAllData=yes
DataTypeSelector=Typ
UsePkg=no

R
R9
R=50 Ohm

VtPulse
SRC4
Vlow=4 V
Vhigh=0 V
Delay=0 nsec
Edge=linear
Rise=0 nsec
Fall=RT_nsec nsec
Width=.5 msec
Period=1 msec

IBIS_Pin
IBISPin3
IbisFile="hc14.ibs"
ComponentName="74HC14_BZ"
PinName="10"
ModelName="HC14_OUTI_33"
SetAllData=yes
DataTypeSelector=Typ
UsePkg=no

R
R8
R=10000 Ohm

VtPulse
SRC7
Vlow=0 V
Vhigh=V_th V
Delay=T_delay_nsec nsec
Edge=erf
Rise=(2.23*RT_nsec) nsec
Fall=RT_nsec nsec
Width=0.5 msec
Period=1 msec

R
R11
R=R_th Ohm

R
R12
R=30 Ohm

VtPulse
SRC2
Vlow=0 V
Vhigh=V_th V
Delay=T_delay_nsec nsec
Edge=erf
Rise=(2.23*RT_nsec) nsec
Fall=RT_nsec nsec
Width=0.5 msec
Period=1 msec

R
R3
R=R_th Ohm

R
R2
R=100 Ohm

VtPulse
SRC8
Vlow=0 V
Vhigh=V_th V
Delay=T_delay_nsec nsec
Edge=erf
Rise=(2.23*RT_nsec) nsec
Fall=RT_nsec nsec
Width=0.5 msec
Period=1 msec

R
R13
R=R_th Ohm

R
R14
R=50 Ohm

VtPulse
SRC9
Vlow=0 V
Vhigh=V_th V
Delay=T_delay_nsec nsec
Edge=erf
Rise=(2.23*RT_nsec) nsec
Fall=RT_nsec nsec
Width=0.5 msec
Period=1 msec

R
R15
R=R_th Ohm

R
R16
R=10000 Ohm
```

Figure 7: Circuit model in ADS for matching Thevenin and IBIS models.

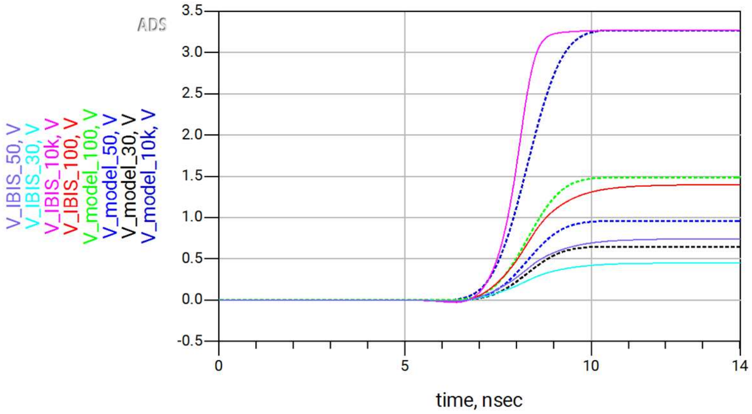


Figure 8: Comparison between Thevenin (dashed lines) and IBIS (solid lines) models. The output impedance of the IBIS model changes based on output load, while the Thevenin model does not. The IBIS model also experiences a shorter rise time under lower loads and has a small amount of ground bounce, suggesting some capacitance in the output and some inductance in the return path.

As the load on the IBIS model of the hex inverter increases, the output voltage decreases due to the output resistance of the device. In this model, the output voltage was set to 3.3 V. The Thevenin model alright, but it has notable limitations. First, the rise time in the IBIS model varied with load, and that is impossible to simulate with a first-order Thevenin model. Second, the Thevenin resistance deviated significantly between loads. Therefore, a Thevenin model would be good under in cases where the load doesn't vary. It's also notable that the IBIS model has a longer rise time and has a bit of ground bounce, implying that the model has some amount of inductance on its return path that the first-order Thevenin model lacks.

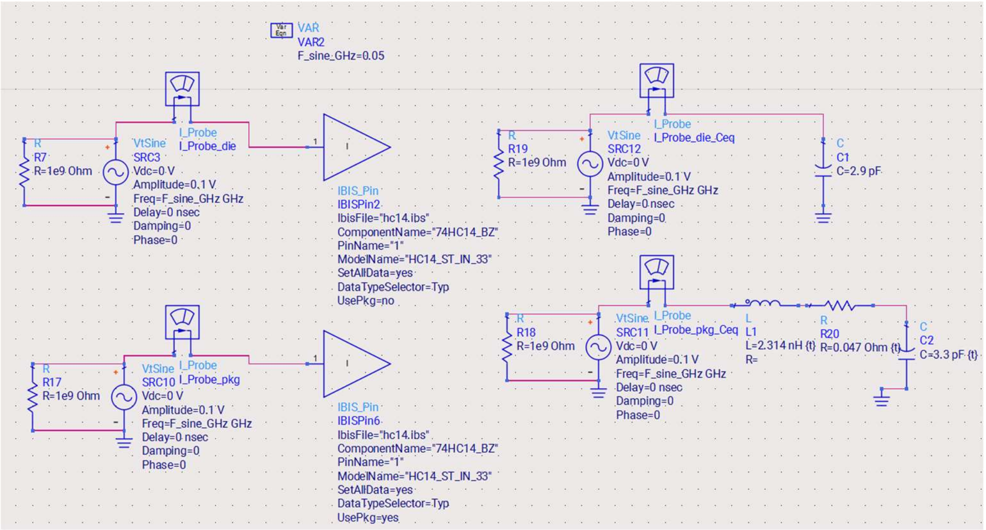


Figure 9: Circuit model in ADS for the input capacitance matching simulations.

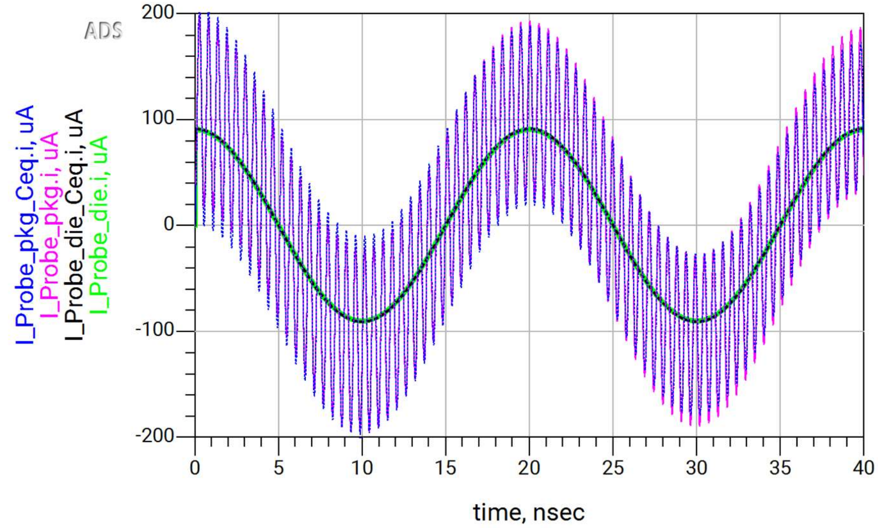


Figure 10: Results from the capacitance matching simulation. The die capacitance (solid green) could be matched very well with a single capacitor (dashed black). Adding the package (solid pink) introduced higher-order harmonics and some resistance that could be modelled by adding inductive and resistive elements (dashed blue), though adding the package had little effect on the input capacitance, increasing it by about 20%.

The input capacitance of the IBIS model is 2.877 pF, which was easily modelled with a lumped capacitance model by adding a capacitor of equivalent size. Adding the package introduced about 0.5 pF of input capacitance, but more notably it added inductive and resistive responses, causing higher-order harmonics.

So what: This lab demonstrated the limitation of first-order Thevenin models. I learned that they shouldn't be trusted for transient analysis if the transients matter. The Thevenin resistance of a power source varies with load, so the Thevenin model should be tuned to match the actual load that the source will experience.

This lab also demonstrated the impact of adding a package to a die, or at least how it affects an IBIS model. I learned that while the package doesn't add a large amount of capacitance, it does have a large impact on the transient performance of the device due to the added inductive and resistive components. In the case of my simulation, the added inductance introduced a higher-order harmonic.