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Week 4 Labs
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Lab 1:

The purpose of this lab is to investigate the effect on impedance in the frequency domain between a single capacitor and a capacitor in parallel with a different capacitance.

The equivalent series inductance (ESL) of both decoupling capacitors is 3 nH, and the equivalent series resistance (ESR) of both decoupling capacitors is 0.01 Ω. The capacitance of the small capacitor is 1 μF and the capacitance for the large capacitor is 10 μF. The self-resonant frequency (SRF) of the capacitors can be calculated by $f_{res} = \frac{1}{2\pi\sqrt{LC}}$, which evaluates to ~1 MHz for the large capacitor and ~3 MHz for the small capacitor.

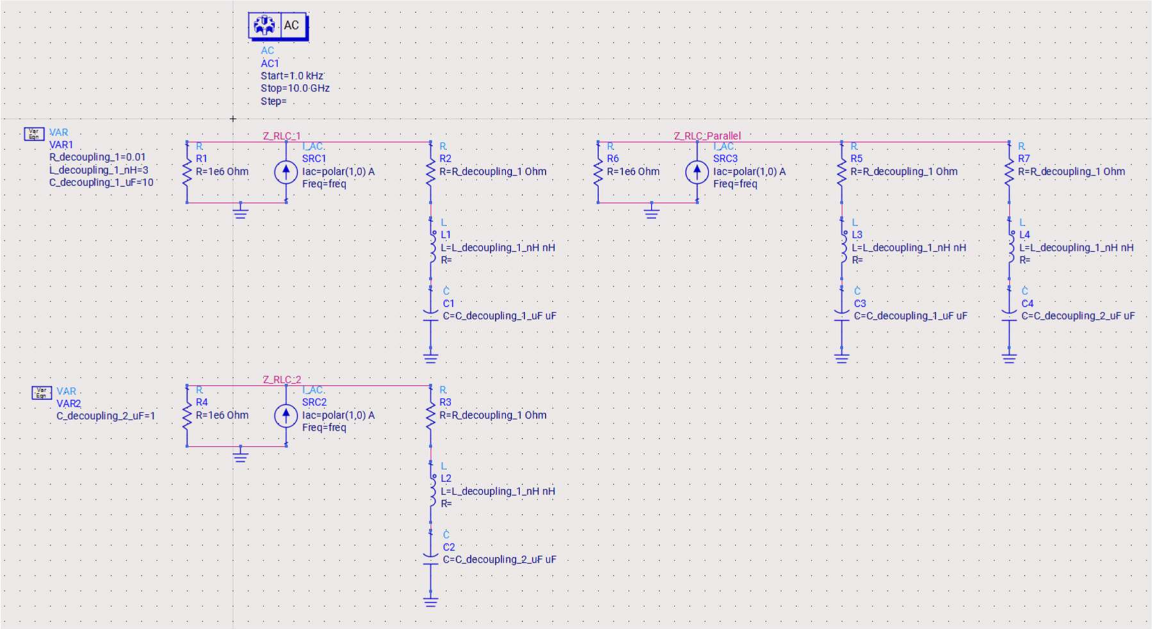

Figure 1: Circuit model in ADS for simulating parallel capacitors.

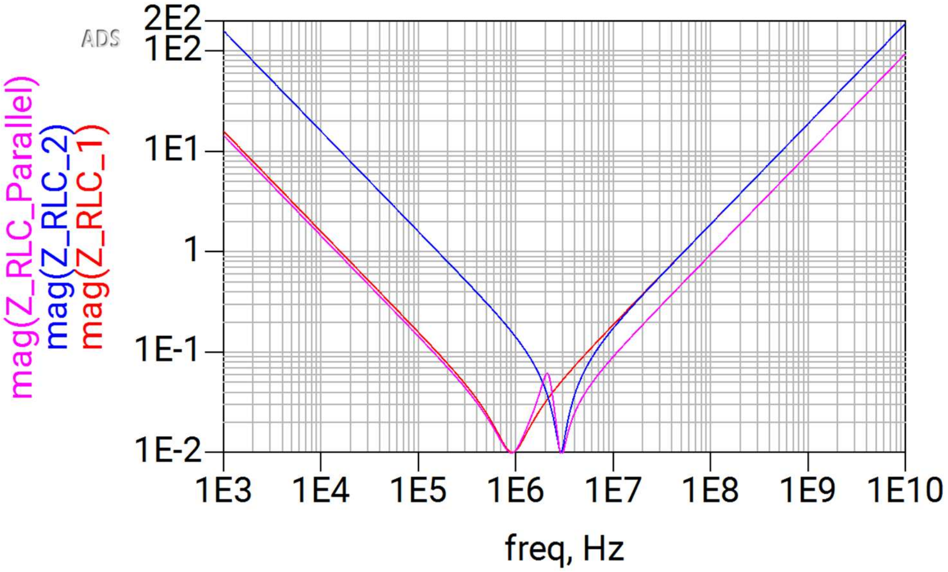

Figure 2: Impedance relative to frequency of the single and parallel capacitor models.

The results for the single capacitors suggest that my estimate for the resonant frequency was accurate because the lowest impedance is ~1 MHz for the large capacitor and ~3 MHz for the small capacitor. The parallel capacitor circuit has low impedances at both resonances. In between the resonant frequencies, the impedance is higher than either single capacitor and it is lower outside of that range.

So what:

These results indicate that smaller capacitors continue to behave like a capacitor up to higher frequencies, which is likely why they are called “high frequency capacitors”. It makes sense that outside of the resonant frequencies, the parallel circuit has a lower impedance than either single-capacitor circuit because the capacitors are acting simply as parallel impedances. In between the resonant frequencies, the impedance has a local peak due to the parallel resonance between the ESL of the large capacitor and the capacitance of the small capacitor. At these frequencies, there will be some resonance, suggesting that we should use only one capacitor when possible to avoid problems from this peak.

Lab 2:

The purpose of this lab is to examine the effect of changing the lead inductance of decoupling capacitors and to investigate how to control the peak of the Bandini Mountain.

The setup for this lab included a series of identical circuits where the only thing being varied is the ESL of the decoupling capacitor. The circuits included on-die capacitance (1 nF) and on-die resistance (1 Ω) for a simulated chip, but lead inductance was ignored. Capacitors were modeled as real capacitors with an ESR of 0.01 Ω and a capacitance of 1 μF. The step current was 100 mA and the 10-90 rise time was 1 ns. Three ESLs were tested, 5 nH, 10 nH, and 1500 nH. The first two are to demonstrate the existence of the Bandini Mountain, and the last one is to demonstrate resonance.

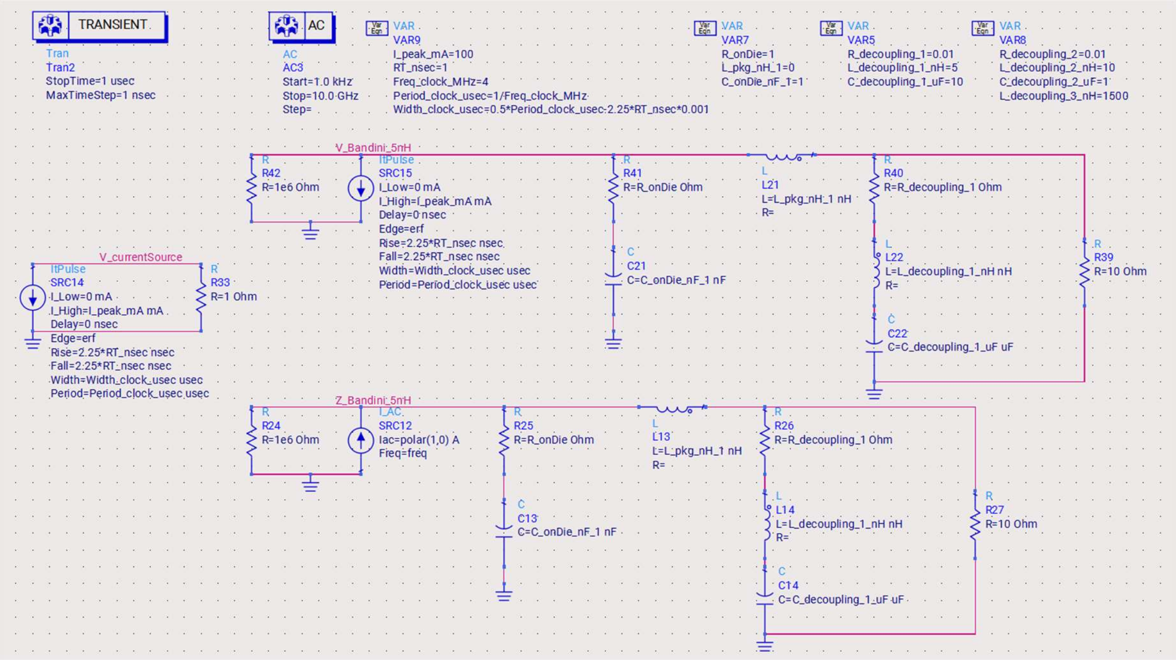

Figure 3: Circuit diagram in ADS for the identical circuits with varying decoupling capacitor ESL. Shown: 5 nH circuit.

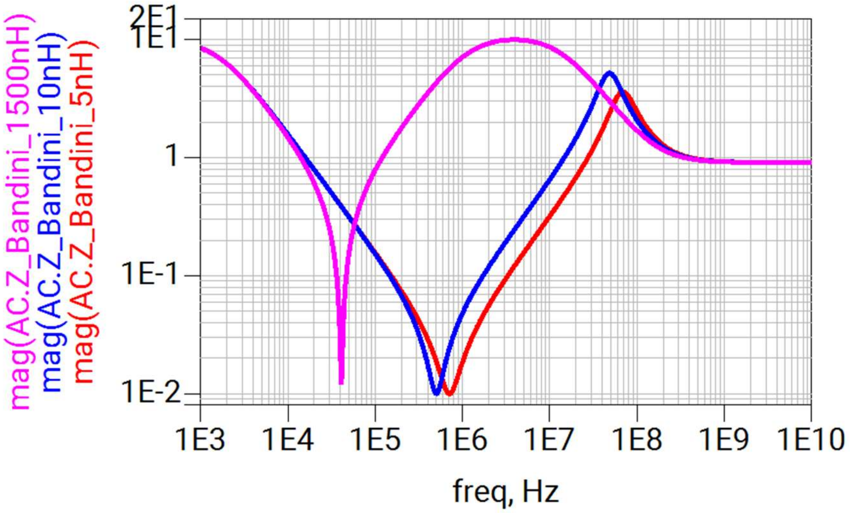

Figure 4: Frequency impedance profile of the simulated chips with high and low impedance. Decoupling capacitor ESL is positively correlated to Bandini peak magnitude and is negatively correlated to Bandini peak frequency.

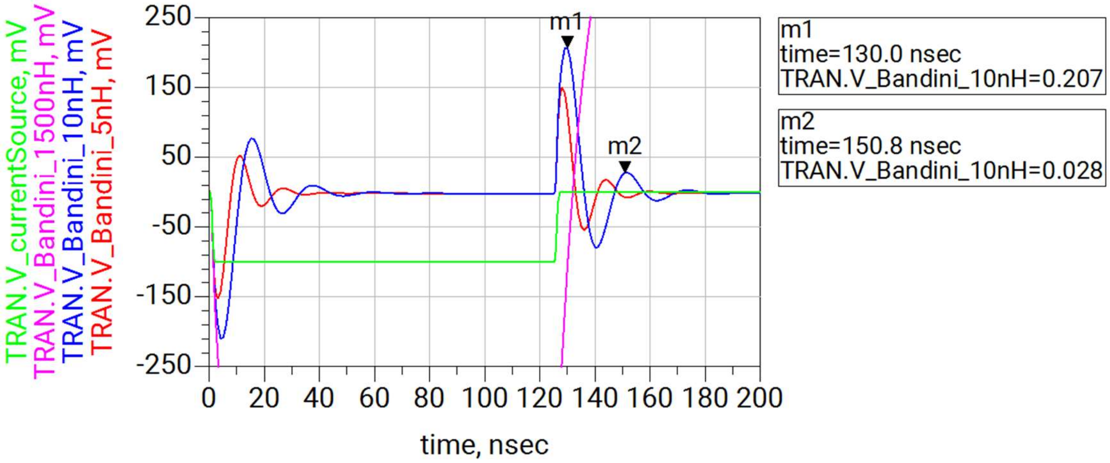

Figure 5: Switching noise of the on-die power rail due to a 100 mA switching load. Decoupling capacitor ESL is inversely proportional with switching noise.

The results from the frequency impedance profile show the lowest impedance for the smaller, realistic inductances is around 170 kHz, and that the Bandini peak is around 50 MHz. This is verified by the transient response of the switching noise, where the 10 nH model exhibits a switching transient with a period of ~20 nsec, or 50 MHz. This is because the high impedance of that frequency means it takes a long time for the frequency to die out after it is hit with a steep edge. The high impedance is due to the resonant frequency between the package capacitance and the decoupling capacitor's ESL.

To exaggerate the effect of resonance, a decoupling capacitor ESL of 1500 nH was simulated so that its Bandini peak is at the frequency of the clock (which is the frequency with the highest-amplitude component frequency). When simulated, the switching noise is off the charts.

<u>So what:</u>

Bandini peaks are unavoidable and those frequencies will be excited. Decreasing the ESL of the decoupling capacitor reduced the magnitude of the peak so that the switching noise attenuates faster. This demonstrates the importance of reducing the ESL of components. In general, this can be done by reducing the footprint of the components so that the loop inductance is smaller. The other component that would affect the magnitude of the Bandini peak is the on-die capacitance, though this is impossible to adjust on-board since it's a property of the silicon chip.

The Bandini peak is due to the parallel resonance between the decoupling capacitor ESL and the on-die capacitance. The capacitance of the decoupling capacitor has no effect on the impedance at high frequencies. Therefore, changing the capacitance of the decoupling capacitor will have no effect on impedance at high frequencies.